National Semiconductor

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CLC730033 Evaluation Boards

Complete Schematic

Figure 1 shows the complete evaluation circuit implemented on this board. The primary connections are shown with solid lines, while several optional circuit connections are shown with dashed lines. Shaded area is inside the device.

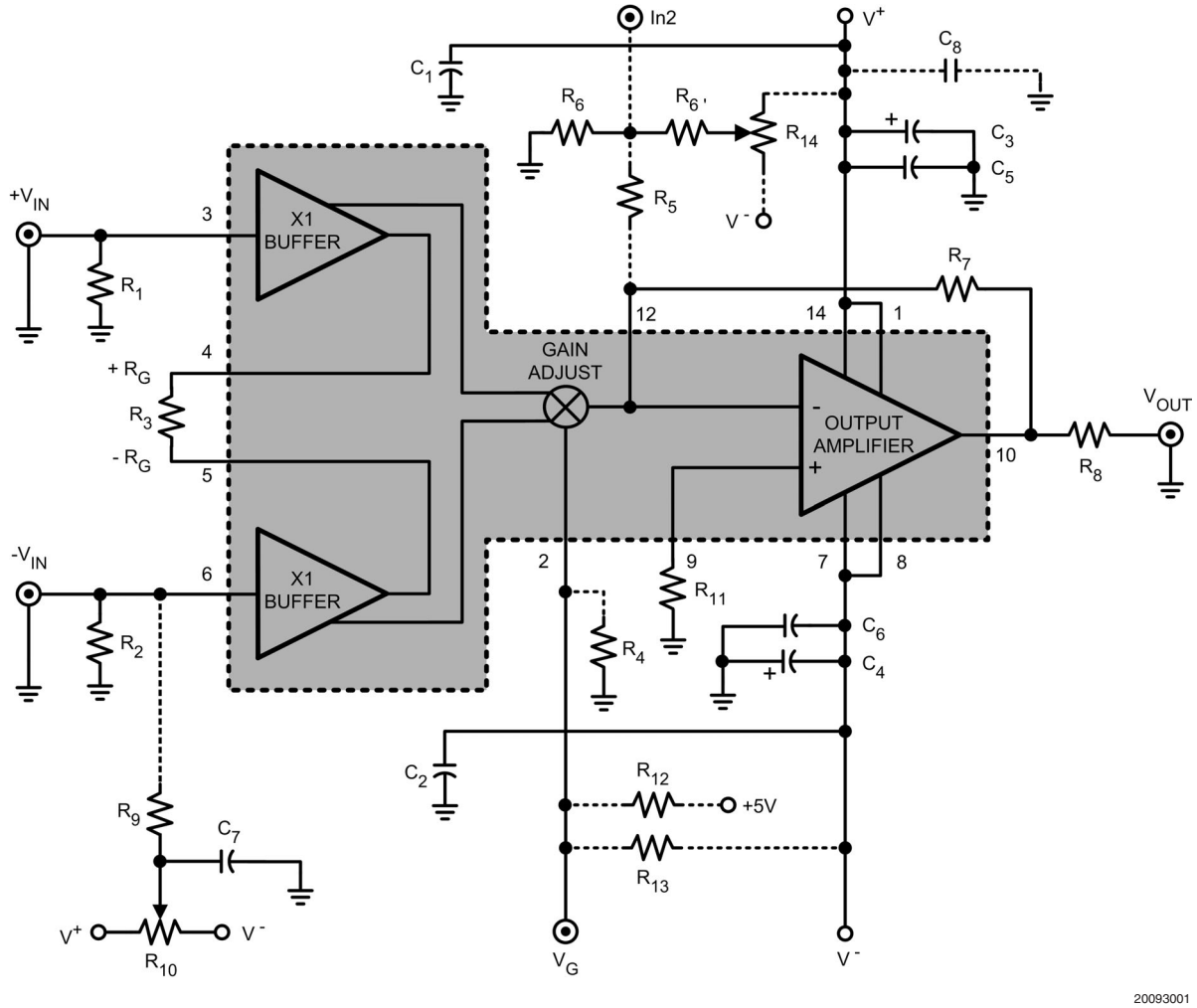

FIGURE 1. External Components & Amplifier Internal Block Diagram

Basic Connection

Figure 2 represents the simplest board configuration. The specific resistor values depicted here configure the device with a maximum gain of 9.9 V/V:

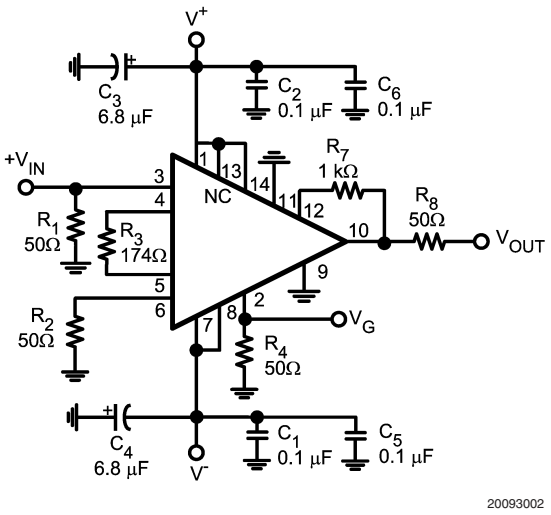

FIGURE 2. Basic Connection

The circuit of *Figure 2* implements a non-inverting variable-gain amplifier with a 50Ω input impedance (R_1), a 50Ω output impedance (R_8), and a maximum gain of 9.9 V/V ($1.72*(R_7/R_3)$). Recognizing the combination of the 50Ω series output resistor and the 50Ω load results in a voltage divider, the gain to this match load is one half of the maximum device gain setting, i.e. 4.9 V/V (13.9 dB). The inverting input (In-) is ground-referenced through 50Ω while the output amplifier's non-inverting input is ground-referenced at pin 9 through R_{11} (not shown, replace R_{11} on board with a short).

Summing Signals and Offsets into the Output Stage

The output amplifier's inverting node (pin 12) is available to introduce any additional signals or offsets into the output. Since pin 12 is a virtual ground, additional signals may be summed into the node without a substantial impact on the signal current flowing from the adjustable-gain path. Briefly, adding an additional impedance on the output amplifier will result in a slight bandwidth reduction of the output amplifier and an increase in the noise gain for the output amplifier's non-inverting input noise voltage. Refer to application note OA-13 for a more thorough discussion of current feedback amplifiers in inverting summing applications. *Figure 3* shows an example of using the optional components on the board to sum in a high-speed signal with a gain of –2 to the output pin (or –1 to the matched 50Ω load).

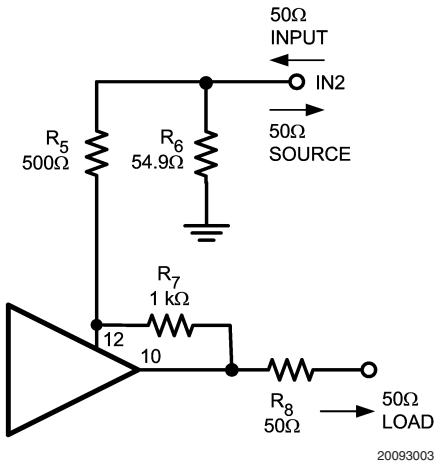

FIGURE 3. Summing a High-Speed Signal Into The Output

Note that R_6 can be used in either of two locations on this board. In*Figure 3* R_6 is positioned as part of the output op amp's inverting input (In2) termination. Alternatively, it can be positioned to pick off the wiper voltage of an offset-adjust pot (R_{14} *Figure 1*) which is to be fed into the inverting node of the output amplifier. *Figure 4* shows this application where an output offset, independent of the gain adjustment stage, is introduced into the inverting node of the output amplifier.

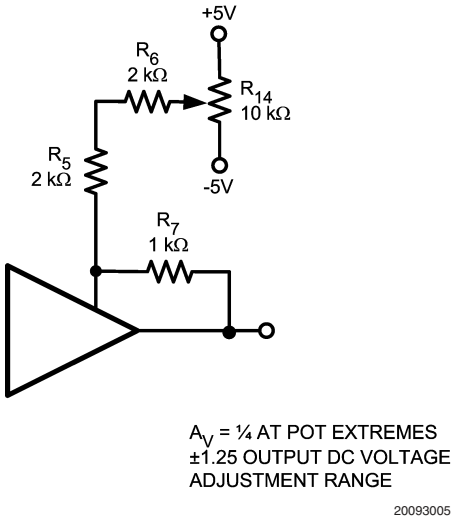

FIGURE 4. Summing in an Output DC Offset

Nulling the Output DC Offset

There are several factors contributing to the output offset voltage; the differential input buffer, the multiplier core and the output amplifier. The offsets produced by the input buffer and the output amplifier can be nulled with appropriate external circuitry. It will not be possible to completely null the offset effects of the multiplier core because of its non-linear nature. As a result, a small non-linear DC offset voltage gain over the adjustment range will always be present at the

Nulling the Output DC Offset

(Continued)

output of the device. *Figure 5* shows the required external circuitry necessary to add the appropriate nulling offsets at both the input buffer and the output amplifier.

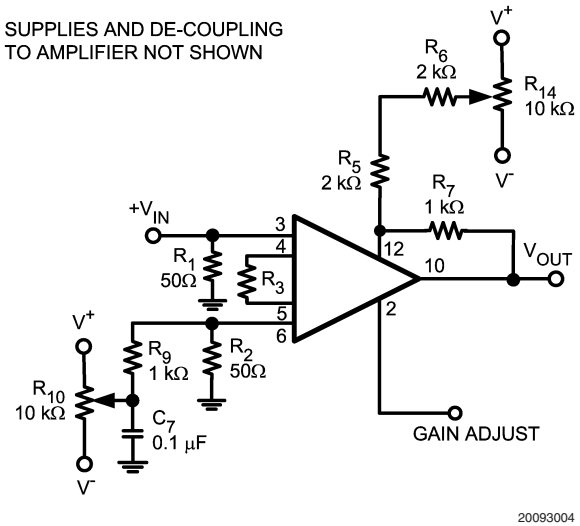

FIGURE 5. Input and Output Stage DC Nulling

The output stage offset should be trimmed prior to the input stage. With the gain adjust pin set at minimum gain (maximum attenuation), the output stage offset may be nulled independently from the input stage. R_{14} should be adjusted to yield the desired output error voltage (typically <1 mV). Having corrected for the input offset voltage and bias current errors of the output amplifier, returning the gain adjust pin to the maximum gain voltage will allow the input buffer stage DC offset errors to be corrected. With no input signal present, but with matched source impedances at each of the two buffer inputs, R_{10} in *Figure 5* can be adjusted to bring the output to within the desired error band.

Adjusting the input and the output stage offsets at the two gain extremes will hold the output DC error at a minimum at these two points in the gain range. If a more limited gain range is anticipated, the adjustments should be made at these operating points. The non-linear DC error introduced by the multiplier core will cause a residual, gain dependent, offset to appear at the output as the gain is swept from minimum to maximum. Also, neither the input nor the output offset adjustment described here will improve temperature drift effects.

Printed Circuit Board Layout

The CLC730033 was designed for evaluation of the CLC520 and CLC522 (obsoleted devices, replaced by the LMH6502 and LMH6503).

There is silk-screen on the board referencing CLC520 and CLC522. *Figure 6* shows both component and circuit side views (gray color depicts the circuit side).

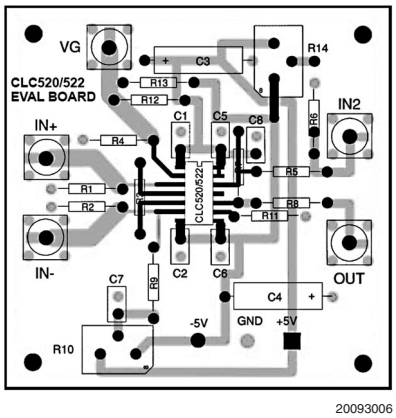

FIGURE 6. CLC730033 (Component and Circuit Side)

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